English Translation of Sho 61-295721

(19) Japanese Patent Office (JP)

(11) Publication Number: Sho 61-295721

(43) Date of publication of application: December 26, 1986

(12) Patent Laid-open Official Gazette (A)

(51) Int.Cl.[4]	Discrimination Mark	JPO file number
H 03 M 1/66		D-6832-5J

The Number of Claims: 4 (8 pages in total)

Request of Examination: not made

(54) Title of the Invention: DIGITAL-ANALOG CONVERTER CIRCUIT

(21) Application number: Sho 61-144017

(22) Date of filing: June 21, Sho 61 (1986)

(71) Applicant: N. V. PHILIPS' GLOEILAMPENFABRIEKEN

Groenewoudseweg 1, NL-5621 BA Eindhoven (NL)

(72) Inventor: Gobert, Jean

130 avenue Gambetta 94700 Maison Alfort FRANCE

(72) Inventor: Michel, Jean-Pierre

6 rue Adele 91330 Yerres FRANCE

(74) Representatives: Patent attorney:

Akihide SUGIMURA and the other.

Specification

1. Title of the Invention

DIGITAL-ANALOG CONVERTER CIRCUIT

2. Scope of Claim

1. A digital-analog converter circuit which affects an accumulator for generating an output signal in accordance with an increment distributed according to a binary weighting scale, and makes a nonlinear response depending on an input code formed of p binary elements B_p for operating M output stages characterized in that:

a converting means is provided, by which an output signal has a property of a segmented nonlinear response;

this segmented nonlinear response is formed of a series of linear segments S_n out of slopes PS_n;

slopes of two consecutive segments have a relation denoted by a following formula: $PS_n + 1 = PS_n + \triangle P_n$; and

here, $\triangle P_n$ maintains the same code for a whole segmented nonlinear response.

2. A digital-analog converter circuit which performs a nonlinear response depending on an input code formed of p binary elements B_p for operating a first portion of M output stages which affect an output signal by an accumulator in accordance with an increment distributed according to a binary weighting scale; which is provided with at least one logic gate for forming a combination of binary elements; and which operates a second portion of the M output stages which affect an output signal by an output of the logic gate, in cooperation with the accumulator, characterized in that:

a converting means is provided, by which an output signal has a property of a segmented nonlinear response;

this segmented nonlinear response is formed of a series of linear segments S_n out of slopes PS_n;

slopes of two consecutive segments have a relation denoted by a following formula: $PS_n + 1 = PS_n + \triangle P_n$; and

here, $\triangle P_n$ maintains the same code for a whole segmented nonlinear response.

3. The digital-analog converter circuit according to claim 1 or 2, characterized in that:

a converting means has a control circuit which generates s digital control signals ($s \geqq 1$) from at least one binary element and a selector which is operated by s digital control signals and shifts all of k least weighted binary elements to k output stages ($k \geqq M - 1$).

4. The digital-analog converter circuit according to claim 3 which relates to claim 2, characterized in that:

a logic gate is an OR gate; and

a segmented nonlinear response of an output signal in the case where a change of a slope $\triangle P_n$ is negative is approximated to a reciprocal of a "gamma" curve of a cathode line display tube by a converting means.

5. The digital-analog converter circuit according to claim 4, characterized in that:

a cathode line display tube is a color tube; and

respective colors of a color signal, red, green and blue are processed by the control circuit.

6. A graphics display device characterized by comprising at least one digital-analog converter circuit according to claim 4 or 5.

7. A TV receiver characterized by comprising at least one digital-analog converter circuit according to claim 4 or 5.

8. The digital-analog converter circuit according to claim 3 which relates to claim 2, characterized in that:

a logic gate is an AND gate; and

a change of a slope $\triangle P_n$ is positive.

3. Detailed Description of the Invention

The present invention relates to a digital-analog converter circuit for affecting an accumulator which generates an output signal in accordance with an increment distributed according to a binary weighting scale and for making a nonlinear response depending on an input code which includes p binary elements B_p which operate M output stages.

Further, the invention relates to a digital-analog converter circuit for making a nonlinear response depending on an input code which includes p binary elements B_p each of which operates a first portion of M output stages affecting an output signal by an accumulator in accordance with an increment distributed according to a binary weighting scale, having at least one logic gate which forms a combination of binary elements, and for operating a second portion of the M output stages affecting the output signal in cooperation with the accumulator by an output of the logic gate.

Furthermore, the invention relates to a TV receiver or a graphic display device which has the digital-analog converter circuit used especially for reproducing a synthetic image.

This kind of circuit is described in a specification of French patent No. 2417901. By this circuit, a means for improving gray scale of a single color signal reproduced from a red signal (R), a green signal (G) and a blue signal (B) is provided so that a property particularly at low luminance is improved. Accordingly, reproduction with high luminance is performed at low luminance by converting a combination of R, G and B color signals that are weighed by a

coefficient.

This circuit does not perform a reproduction process of a single color gray scale corresponding to each of R, G and B color signals by reproduction proportional to an input code. This can be performed only by considering a parameter generally called "a gamma curve of a display tube".

An object of the invention is reproducing a single color luminance which changes linearly with an arbitrary input code corresponding to each luminance of R, G and B color signals. In this case, the "gamma" curve of the display tube is required to be considered.

Another object of the invention is providing a low-cost digital-analog converter circuit simply constituted to perform enlargement of the converter circuit depending on the number of binary elements P of an input code, in which a response curve thereof approximates to a reciprocal of the "gamma" curve of the display tube.

Another object of the invention is providing a digital-analog converter circuit in which change of an output signal by a digital input code can approximate to a curve having a rise or fall slope by a series of segments.

According to the invention, in a digital-analog converter circuit for affecting an accumulator generating an output signal in accordance with an increment distributed according to a binary weighting scale and for making a nonlinear response depending on an input code formed of p binary elements B_p for operating M output stages, a converting means by which an output signal is to have a property of a segmented nonlinear response is provided, wherein the segmented nonlinear response is provided, wherein the segmented nonlinear response is formed of a series of linear segments S_n on slopes PS_n, and slopes of two consecutive segments have a relation expressed by a following formula: $PS_n + 1 = PS_n + \triangle P_n$ in which $\triangle P_n$ maintains a same code corresponding to a whole segmented nonlinear response.

In implementation of the invention, a converting means is provided with a control circuit for generating s digital control signals ($s \geqq 1$) from at least one binary element, and a selector for shifting all k least weighted binary elements to k output stages ($k \geqq M - 1$), which is operated by s digital control signals.

By s control signals supplied from the control circuit, 2^s conversions are performed at the selector. Accordingly, an approximation of a curve is performed by 2^s segments.

Therefore, the desired maximum number of output stages is p + s, by which 2^s segments can be covered.

In the case where the converter circuit has a logic gate which operates a second portion of M output stages, all levels of an output signal overlapped with segmentalization into 2^s segments obtained by using s digital control signals can be shifted.

By these logic gates, one of the M output stages is operated. In the case where the logic gate is an OR gate, approximation of a curve that a change of a slope $\triangle P_n$ is negative can be performed. Further, in the case where the logic gate is an AND gate, approximation of a curve that a change of a slope $\triangle P_n$ is positive can be performed.

The invention can be applied particularly to an approximation of a reciprocal of a "gamma" curve of a cathode line display tube.

A cathode line color receiving tube has a luminance conversion response property of a nonlinear control voltage-fluorescent material. Three control voltages are converted in accordance with a following formula: $Y = k \cdot v\gamma$ by three electric guns. Here, v denotes an image luminance signal, Y denotes a luminance and k denotes a constant.

The three electric guns of a color tube make almost a same response respectively under the condition that an exponent is 1.5 to 3. Making a nonlinear response in this way means that a control signal is required to be corrected in advance by supplying a brightness signal $v' = v^{1/\gamma}$ to a TV receiver or a display device.

Such correction of supplying each of three electric guns of original colors R, G and B can be performed with a converter circuit of the invention.

In a preferred example of the invention, a slope approximates by three segments on which slopes are reduced as luminance increases.

A code is formed of four binary elements (p = 4) and p + 2 stages are formed by current sources distributed in accordance with binary weights: 1/2, 1/4, 1/8, 1/16, 1/32 and 1/4.

Further, a luminance of 0 and a high luminance correspond to 0000 and 1111, respectively.

In order to obtain these three segments, according to the invention, a multiplexing process is performed for less weighted binary elements, B_1, B_2 and B_3 using a most weighted binary element B_4. That is to say,

the current source 1/2 is operated by B_4.

the current source 1/4 or 1/8 is operated by B_3.

the current source 1/8 or 1/16 is operated by B_2.

the current source 1/16 or 1/32 is operated by B_1.

$B_4 = 0$ is obtained thereby.

the current source 1/2 is not operated by B_4.

the current source 1/4 is operated by B_3.

the current source 1/8 is operated by B_2.

the current source 1/16 is operated by B_1.

$B_4 = 1$ is obtained thereby.

the current source 1/2 is not operated by B_4.

the current source 1/8 is operated by B_3.

the current source 1/16 is operated by B_2.

the current source 1/32 is operated by B_1.

The current source 1/4 is operated by a logic OR gate connected to the binary elements B_1, B_2, B_3 and B_4 in order to increase low level luminance. Therefore, there are advantages that a "gamma" curve is approximated well and a required change of a current source is used. This value is changed and this is not required to correspond to a binary weight.

A single color gray scale can be obtained as is shown in a following table I by the converter circuit. Accordingly, a satisfactory curve which approximates to a gamma curve of a conventional cathode line tube can be obtained.

Table I

Code		Output (I)
0	0	0
1	10/32	5/16
2	12/32	3/8
3	14/32	7/16
4	15/32	1/2
5	18/32	9/16
6	20/32	5/8

7	22/32	11/16
8	24/32	3/4
9	25/32	25/32
10	26/32	13/16
11	27/32	27/32
12	28/32	7/8
13	29/32	29/32
14	30/32	15/16
15	31/32	31/32

Such digital-analog converter circuit is easily formed and economical. According to the invention, good approximation of a curve can be obtained by operating a large number of binary elements, for example, five binary elements with 32 unit steps. In addition, lots of control signals can be obtained with the control circuit, thereby the selector can be operated and an increment or a decrement of a slope which is almost a curve can be obtained.

The invention is described with reference to drawings.

In a digital-analog converter circuit of the invention shown in FIG. 1, a register 11 is provided, which includes binary elements of p = 4. The register 11 is connected to a selector 13 and a control circuit 14, thereby s digital control signals for controlling the selector 13 are supplied to an output conductive line 16. A converting means 18 is formed by the selector 13 and the control circuit 14. In a first embodiment of the invention, a logic gate for directly operating an output stage 12 is not provided in the converting means 18. The selector 13 is connected to the output stage 12, and the number of the output stages 12 is $p + 2^s - 1$ in this embodiment. These output stages 12 are connected to an accumulator 15, from which an output signal of the digital-analog converter circuit is generated. A curve which indicates the output signal is divided into 2^s segments by setting the number of digital control signals to s.

An operation mechanism of the selector 13 which relates to a second embodiment of the invention is shown in detail in FIG. 2. A logic gate for directly operating the output stage 12 connected also to the accumulator 15 is provided in the abovementioned converting means 18 in this embodiment.

The control circuit 14 receives five binary elements B_1 to B_5 from the register 11.

Here, B_1 is a least weighted binary element, and B_5 is a most weighted binary element. There are 32 possible combinations as an input code by using five binary elements. A current can be supplied in accordance with a binary weight by the output stage 12 connected to the selector 13. A control signal for operating the selector 13 is generated by the control circuit 14, and thus the selector shifts outputs of the register 11 all at once and supplies these outputs to current sources arranged in binary weight sequential ascending (or descending) order. These shifts which affect some or all binary elements of the register 11 can be repeated using 2^5 possible combinations. Some of 2^5 possible combinations are required to be used depending on a shape of a curve to approximate. At a slope in which an exponent of two is changed, digital control signals C1, C2 and C3 are generated by the control circuit 14 so as to approximate a gamma curve of a display tube by using four segments, under the following condition.

$$C1 = \overline{B_4 + B_5}, \quad C2 = \overline{B_5}, \quad C3 = \overline{B4 \cdot B5}$$

Here, a mark (+) denotes a logic OR function, a mark ($\cdot$) denotes a logic AND function, and a mark ($\bar{}$) denotes a logic " inverted " function.

In the case where the digital control signal C1, C2 or C3 is in a logical state of "0", the selector is set by these control signals so that these selectors are controlled on the upper side in FIG. 2. Alternatively, in the case where the digital control signal C1, C2 or C3 is in a logical state of "1", the selector is set by these control signals so that these are controlled on the bottom side in FIG. 2. Following current sources I, 2I, 4I, 8I, 16I, 32I, 64I and 96I are operated in accordance with an output of the selector. Here, a value I denotes a unit current increment. All of these output signals showing a segmented curve can be shifted. This shift is performed by operating one or more current sources by using one or more logic gates 20. A value of a logic gate Id is determined in accordance with amplitude of a shift to be obtained.

As an economical and preferred embodiment of the invention, a simple digital-analog converter circuit is shown in FIG. 3, which is constituted by input codes of four binary elements and one logic OR gate.

In this embodiment, four binary elements of an input code are memorized in the register 11. Further, the output stage 12 is constituted by six stages in total which increase an output signal in accordance with a binary weight. This output stage is constituted by six current generating apparatuses with weights 1/2, 1/4, 1/8, 1/16, 1/32 and 1/4, respectively. Binary

elements B_1, B_2 and B_3 are directed all at once to various current sources for a predetermined time, by the selector 13 controlled by the most weighted binary element B_4. That is to say,

the current source 1/4 or 1/8 is controlled by B_3.

The current source 1/8 or 1/16 is controlled by B_2.

The current source 1/16 or 1/32 is controlled by B_1.

The logic OR gate generates a signal for controlling another current source, for example, 1/4, corresponding to the binary elements, B_1, B_2, B_3 and B_4. The current source1/2 is controlled by the binary element B_4.

Outputs of six output stages 12 are supplied to the accumulator 15 to accumulate various output currents, thereby an adequate circuit of a TV receiver or a graphic display device is operated.

A more specific configuration of the selector 13 is shown in FIG. 4. That is to say, the selector 13 includes an inverting switch 21 for generating an inverted signal $\overline{B_4}$ of an input signal B_4; an AND gate 22 for receiving signals B_4 and B_3; an AND gate 23 for receiving signals $\overline{B_4}$ and B_3; an AND gate 24 for receiving signals B_4 and B_2; an AND gate 25 for receiving signals $\overline{B_4}$ and B_2; an AND gate 26 for receiving signals B_4 and B_1; an AND gate 27 for receiving signals $\overline{B_4}$ and B_1; an OR gate 28 for receiving outputs of the AND gates 23 and 24; and an OR gate 29 for receiving outputs of the AND gates 25 and 26.

Six output stages 12 formed of six current sources are controlled as described in the following.

The current source 1/2 is controlled by the signal B_4.

The current source 1/4 is controlled by an output of the AND gate 22.

The current source 1/8 is controlled by an output of the OR gate 28.

The current source 1/16 is controlled by an output of the OR gate 29.

The current source 1/32 is controlled by an output of the AND gate 27.

Accordingly, a control signal is constituted by an inverted value $\overline{B_4}$ which is supplied from the binary element B_4 and the inverting switch 21.

The selector 13 of FIG. 4 is configured as described above. Alternately, this selector can be configured by a simple transistor in accordance with a technique which is used, for example, in a MOS technique. Therefore, in this case, the transistor works as a transfer element

controlled by the signal B_4 or $\overline{B_4}$.

FIG. 5 shows a response curve 31 of the converter circuit of the invention by four codes of binary elements. This curve particularly approximates to a "gamma" curve 32 of a cathode line tube having a coefficient r = 1.5.

FIG. 6 shows two response curves of the converter circuit of the invention by five codes of binary elements shown in FIG. 2. That is to say, a curve 61 is an approximating curve of a "gamma" curve, which is formed of four segments the slope of which descends at a rate of an exponent of two. This curve is formed by a circuit of FIG. 2 in the case where there is no logic gate 20, therefore, the current source Id is not operated. On the other hand, although a curve 62 is formed of four segments the slope of which descends at a rate of an exponent of two, and shows an approximation of a "gamma" curve, the curve 61 is shifted at an origin in the first segment, in this case. This shift can be performed using a logic OR gate having five input terminals by operating the current source Id, when one of five input binary elements is in a state of logical "1". An output signal of a digital-analog converter circuit which approximates to a gamma curve of a display tube adapts to a normal circuit of a display tube in which a normal amplified circuit is used.

Three original colors, red, green and blue of a normal cathode line tube display device are processed respectively, using three abovementioned digital-analog converter circuits of the invention. Therefore, although there are 16 shadow gray scale levels by four codes of binary elements for respective colors, this gray scale level can be easily increased to 32, 64, ..., by adding 1, 2, ..., plurality of additional binary elements. This color gray scale can be used for reproducing a synthetic image in particular obtained by a computer process. An extremely broad range of gray scales for intensity of respective colors is required to reproduce an image faithfully in this manner. The converter circuit of the invention can perform image reproduction easily even in the case of four or more input codes of binary elements.

The abovementioned digital-analog converter circuit can be formed by using a normal digital-analog converter having a multiplexer and an OR gate. It is preferable that all of these circuit elements are integrated to configure a single converter circuit for reduction in its cost.

The invention is described as approximation of a $v^{1/\gamma}$ type curve in the case where $1/\gamma \simeq 0.66$. Alternately, it can be approximated to a v^{β} type curve in the case of ß 1.5, using a

complete equivalent circuit. In this case, a weight of a current source of the output stage 12 is required to be changed as is shown in FIG. 7. That is to say, the binary elements B_1, B_2 and B_3 are supplied to the selector 13 by the register 11 to operate a current source of a weighting coefficient 1/4 by the most weighted binary element B_4. The selector 13 is connected to current sources of values, that is, weighting coefficients 1/4, 1/8, 1/16 and 1/32 respectively. The selector 13 is controlled by the binary element B_4, thereby two possible combinations of the binary elements B_1, B_2 and B_3 are shifted. In this embodiment, the binary elements B_1, B_2 and B_3 are shifted to the least weighted current source in the case where the binary element B_4 is in a state of logical "0", and these binary elements are shifted to the most weighted current source in the case of the opposite state, unlike the case of a circuit which approximates to $v^{1/\gamma}$ in the case where $1/\gamma \simeq 0.66$. A logic AND gate 14' generates an output signal inputting four binary elements, and a current source of a weighting coefficient 1/4 is operated by this signal. The value of this weighting coefficient is not required to be the value according to a binary weight. Therefore, ß 1.5 is provided, that is to say, approximation of a $v^{ß}$ type curve can be obtained on an increasing slope P_n. In this case, a change of the slope $\triangle P_n$ is constantly positive.

4. Brief Description of the Drawings

FIG. 1 is a block circuit diagram showing an embodiment of a digital-analog converter circuit of the invention in the case where no logic gate for directly operating an output stage directly is included.

FIG. 2 is a block circuit diagram showing another embodiment of a digital-analog converter circuit of the invention in the case where a logic gate for directly operating an output stage is included.

FIG. 3 is a block circuit diagram showing another example of a converter circuit of the invention in the case where approximation of a reciprocal of a "gamma" curve of a display tube is performed.

FIG. 4 is a circuit diagram showing a detailed arrangement of a connection of a selector shown in FIG. 3.

FIG. 5 is a characteristic diagram showing shapes of a "gamma" curve and an approximation curve obtained from an output signal of the converter circuit of FIG. 3.

FIG. 6 is a characteristic diagram showing shapes of an approximation curve obtained from an output signal of the converter circuit of FIG. 2 in the case where a logic gate for directly operating an output stage is provided and it is not provided.

FIG. 7 is a block circuit configuration showing another embodiment of a converter circuit of the invention in the case of approximation of a curve having a positive change of a slope.

11...	register	12...	output stage
13...	selector	14...	control circuit
14'...	logic AND gate	15...	accumulator
16...	conductive line	18...	converting means
21...	invert switch	22 to 27...	AND gates

28 and 29...OR gates